SPECIFICATION
FOR
LCD Module
KD035HVFMD057-CTP-005

MODULE:	KD035HVFMD057-CTP-005
CUSTOMER:	

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CHECKED BY		
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Contents

1. Block Diagram 5
2. Outline dimension 6
3. Input terminal Pin Assignment 7
3.1 TFT 7
3.2 CTP 9
4. LCD Optical Characteristics 10
4.1 Optical specification 10
5. Electrical Characteristics 12
5.1 Absolute Maximum Rating (Ta=25 VSS=0V) 12
5.2 DC Electrical Characteristics 12
5.3 LED Backlight Characteristics 13
6. AC Characteristic 15
6.1 Display Parallel 8/16-bit Interface Timing Characteristics (8080 system) 15
6.2 Display Serial Interface Timing Characteristics (3-line SPI system) 17
6.3Display Serial Interface Timing Characteristics (4-line SPI system) 18
6.4 Parallel RGB Interface Timing Characteristics 19
6.5 Reset Timing Characteristics 21
7. CTP Specification 22
7.1 Electrical Characteristics 22
7.1.1 Absolute Maximum Rating 22
7.1.2 DC Electrical Characteristics (Ta=25℃) 22
7.2 AC Characteristics 23
7.2.1 I2C Interface 23
8.LCD Module Out-Going Quality Level 25
8.1 VISUAL & FUNCTION INSPECTION STANDARD 25
8.1.1 Inspection conditions 25
8.1.2 Definition 25
8.1.3 Sampling Plan 26
8.1.4 Criteria (Visual) 27
9. Reliability Test Result 31
9.1 Condition 31
10. Cautions and Handling Precautions 32
10.1 Handling and Operating the Module 32
10.2 Storage and Transportation. 32
11. Packing 33

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 3.5'TFT-LCD contains 320x480 pixels, and can display up to 65K/262K colors.

* Features

-Low Input Voltage: 3.3V(TYP)

-Display Colors of TFT LCD: 65K/262K colors

-TFT Interface: 8/9/16/18Bit MCU Interface
3/4SPI+16/18Bit RGB Interface
3-line/4-line Serial Interface

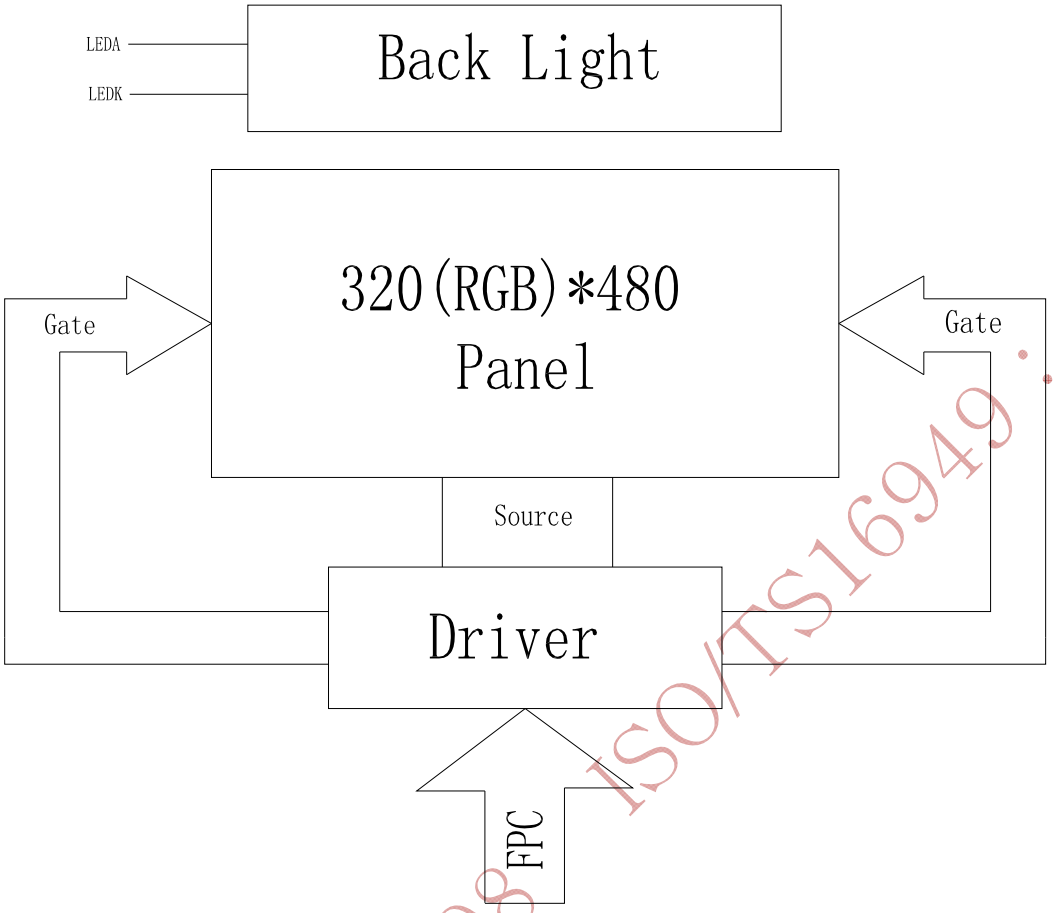
-CTP Interface: I2C

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	48.96(H)*73.44（V） (3.5inch)	mm	-
CTP View area	49.96(H)*74.44(V)	mm	
Driver element	TFT active matrix	-	-
Display colors	65K/262K	colors	-
Number of pixels	320(RGB)*480	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.153(H)*0.153(V)	mm	-
Viewing angle	ALL	o'clock	-
TFT Controller IC	ILI9488	-	-
CTP Driver IC	FT6236		
Display mode	Transmissive/Normally Black	-	-
Touch mode	Single point and Gestures		
Operating temperature	-20～+70	℃	-
Storage temperature	-30～+80	℃	-

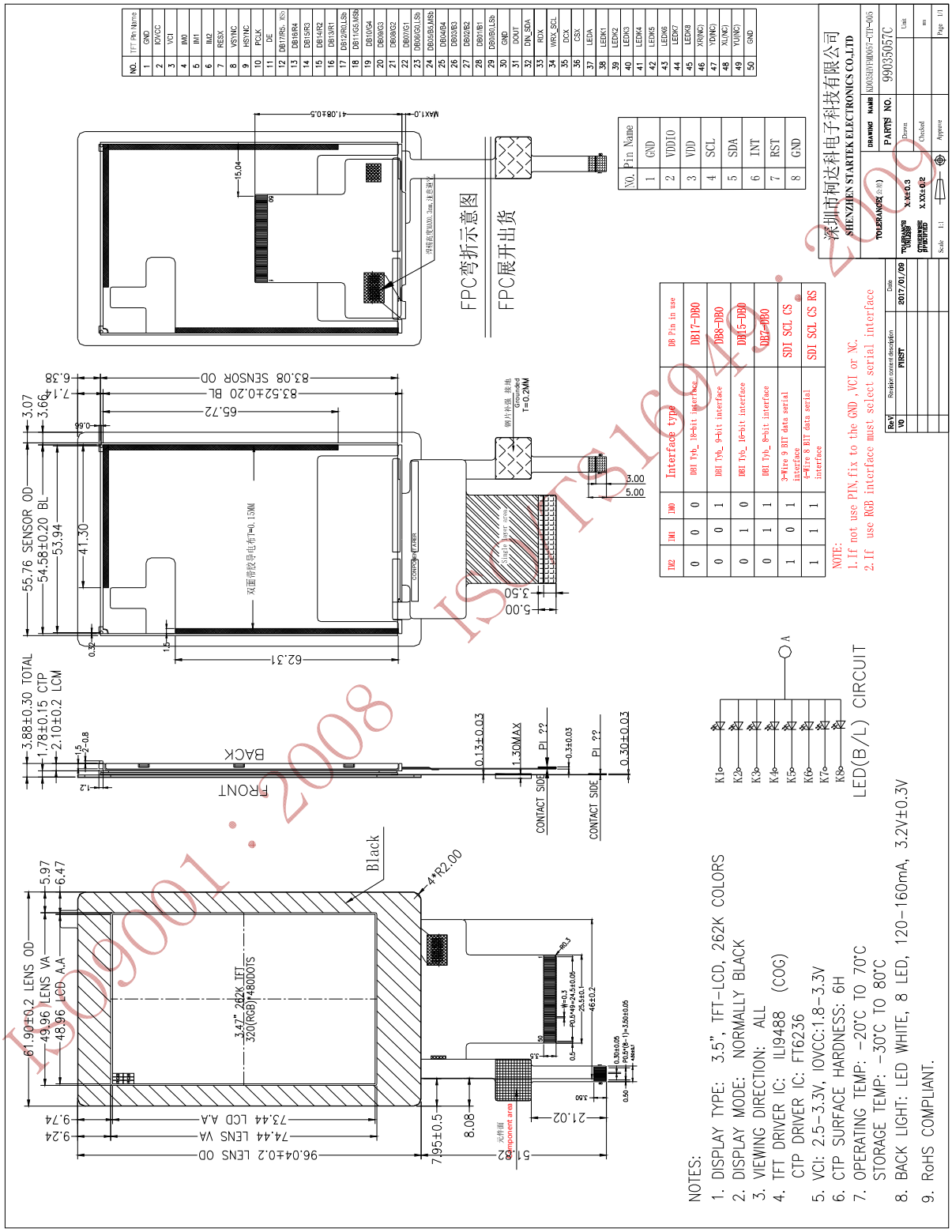
* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		61.90		mm	-
	Vertical(V)		96.04		mm	-
	Depth(D)		3.88		mm	-
Weight			TBD		g	-

1. Block Diagram



2. Outline dimension



3. Input terminal Pin Assignment

3.1 TFT

<table>
<tr><th>NO.</th><th>SYMBOL</th><th>DISCRIPTION</th><th>I/O</th></tr>
<tr><td>1</td><td>GND</td><td>Ground.</td><td>P</td></tr>
<tr><td>2</td><td>IOVCC</td><td>Supply voltage for IO(1.8-3.3V)</td><td>P</td></tr>
<tr><td>3</td><td>VCI</td><td>Supply voltage(3.3V).</td><td>P</td></tr>
<tr><td>4</td><td>IM0</td><td rowspan="6">
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface type</th><th>DB Pin in use</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>DBI Tyb_ 18-bit interface</td><td>DB17-DB0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>DBI Tyb_ 9-bit interface</td><td>DB8-DB0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>DBI Tyb_ 16-bit interface</td><td>DB15-DB0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DBI Tyb_ 8-bit interface</td><td>DB7-DB0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3-Wire 9 BIT data serial interface</td><td>SDA SCL CS</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>4-Wire 8 BIT data serial interface</td><td>SDA SCL CS RS</td></tr>
</table>
</td><td rowspan="6">I</td></tr>
<tr><td>5</td><td>IM1</td></tr>
<tr><td>6</td><td>IM2</td></tr>
<tr><td>7</td><td>RESX</td><td>This signal will reset the device and must be applied to properly initialize the chip.</td><td>I</td></tr>
<tr><td>8</td><td>VSYNC</td><td>Frame synchronizing signal for RGB interface operation.
fix this pin at VCI or GND when not in use.</td><td>I</td></tr>
<tr><td>9</td><td>HSYNC</td><td>Line synchronizing signal for RGB interface operation.
fix this pin at VCI or GND when not in use</td><td>I</td></tr>
<tr><td>10</td><td>PCLK</td><td>Dot clock signal for RGB interface operation
Fix this pin at VCI or GND when not in use.</td><td>I</td></tr>
<tr><td>11</td><td>DE</td><td>Data enable signal for RGB interface operation.
fix this pin at VCI or GND when not in use.</td><td>I</td></tr>
<tr><td>12-29</td><td>DB17-DB0</td><td>18-bit parallel bi-directional data bus for MCU system and RGB interface mode .
Fix to GND level when not in use</td><td>I/O</td></tr>
<tr><td>30</td><td>GND</td><td>Ground.</td><td>P</td></tr>
<tr><td>31</td><td>DOUT</td><td>Serial data output pin in serial bus system interface.
If not used, please open this pin.</td><td>O</td></tr>
<tr><td>32</td><td>DIN_SDA</td><td>Serial input signal.The data is applied on the rising edge of the SCL signal.
If not used, fix this pin at VCI or GND.</td><td>I</td></tr>
<tr><td>33</td><td>RDX</td><td>Serves as a read signal and MCU read data at the rising edge.
fix this pin at VCI or GND when not in use.</td><td>I</td></tr>
</table>

34	WR(SPI-SCL)	DBI Type B: WRX pin, serves as a write signal DBI Type C: SCL pin as Serial Clock when operates in the serial interface	I
35	DCX(RS)	Display data/ command selection pin	I
36	CSX	Chip select input pin (“Low” enable). fix this pin at VCI or GND when not in use.	I
37	LEDA	Anode pin of backlight	P
38	LEDK1	Cathode pin OF backlight	P
39	LEDK2	Cathode pin OF backlight	P
40	LEDK3	Cathode pin OF backlight	P
41	LEDK4	Cathode pin OF backlight	P
42	LEDK5	Cathode pin OF backlight	P
43	LEDK6	Cathode pin OF backlight	P
44	LEDK7	Cathode pin OF backlight	P
45	LEDK8	Cathode pin OF backlight	P
46	XR(NC)	Touch panel Right Glass Terminal	A/D
47	YD(NC)	Touch panel Bottom Film Terminal	A/D
48	XL(NC)	Touch panel LIFT Glass Terminal	A/D
49	YU(NC)	Touch panel Top Film Terminal	A/D
50	GND	Ground.	P

3.2 CTP

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	VDDIO	I/O power supply voltage.	P
3	VDD	Supply voltage.	P
4	SCL	I2C clock input.	I
5	SDA	I2C data input and output	I/O
6	INT	External interrupt to the host.	I
7	RST	External Reset, Low is active.	I
8	GND	Ground.	P

4. LCD Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	Θ=0 Normal viewing angle	--	500	--		NOTE2
Response time	Rising	$T_{R+}T_F$		--	35	50	msec	NOTE4
	Falling							
Uniformity		S(%)		--	70	--	%	NOTE1
Color Filter Chromacicity	White	W_X		--	0.301	0.303		
		W_Y		--	0.335	0.337		
	Red	R_X		--	0.631	0.633		
		R_Y		--	0.334	0.335		
	Green	G_X		--	0.316	0.318		
		G_Y		--	0.602	0.605		
	Blue	B_X		--	0.151	0.152		
		B_Y		--	0.047	0.049		
Viewing angle	Hor.	Θ_L	CR>10	--	80	--		NOTE5
		Θ_R		--	80	--		
	Ver.	Θ_U		--	80	--		
		Θ_D		--	80	--		
Option View Direction		Free						

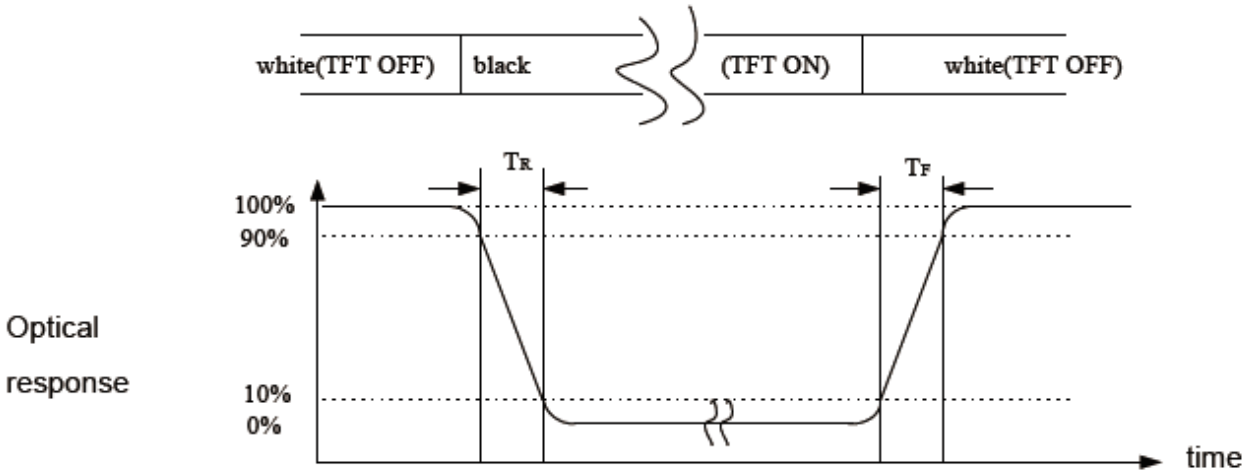
Note 1 Uniformity

$$\text{Uniformity of 9 points} = \frac{\text{Min Luminance of Y1~Y9}}{\text{Max Luminance of Y1~Y9}} \times 100\%$$

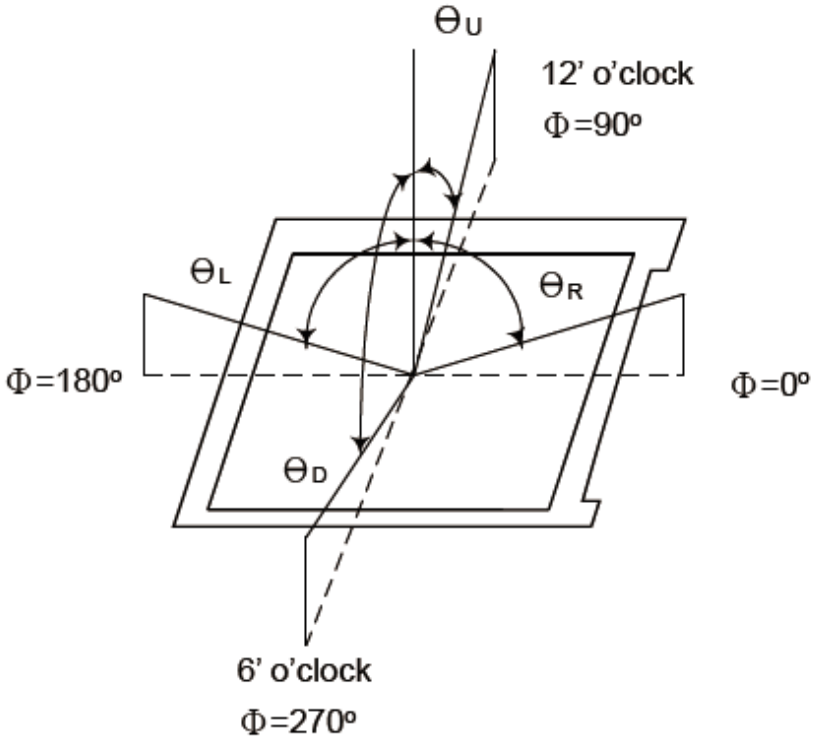
Note 2 Contrast Ratio（CR）

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note 4 Response Time



Note 5 View Angle



5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VCI/VDD	-0.3	4.6	**V**
Digital interface supple Voltage	IOVCC	-0.3	4.6	**V**
Operating temperature	T_{OP}	-20	+70	℃
Storage temperature	T_{ST}	-30	+80	℃

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCI/VDD	2.4	2.8	3.3	V	
Digital interface supple Voltage	IOVCC	1.65	1.8	3.3	V	
Normal mode Current consumption	IDD	--	7	--	mA	
Level input voltage	V_{IH}	0.7V_{DDIO}		VDDIO	V	
	V_{IL}	GND		0.3V_{DDIO}	V	
Level output voltage	V_{OH}	0.8VDDIO		VDDIO	V	
	V_{OL}	GND		0.2VDDIO	V	

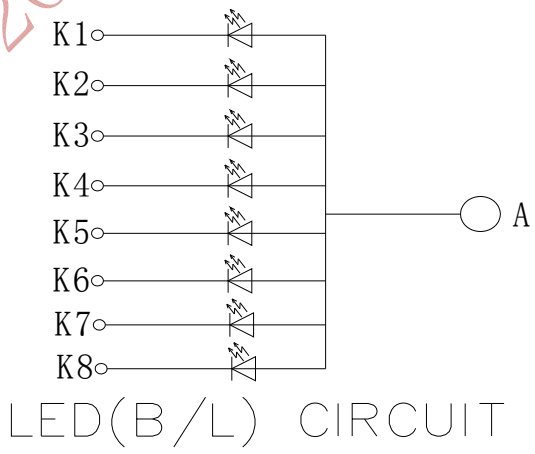
5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 8 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	150	160	--	mA	
Forward Voltage	V_F	--	3.2	--	V	
LCM Luminance	L_V	450	--	--	cd/m2	Note3
LED life time	Hr	50000	--	--	Hour	Note1,2
Uniformity	AVg	80	--	--	%	Note3

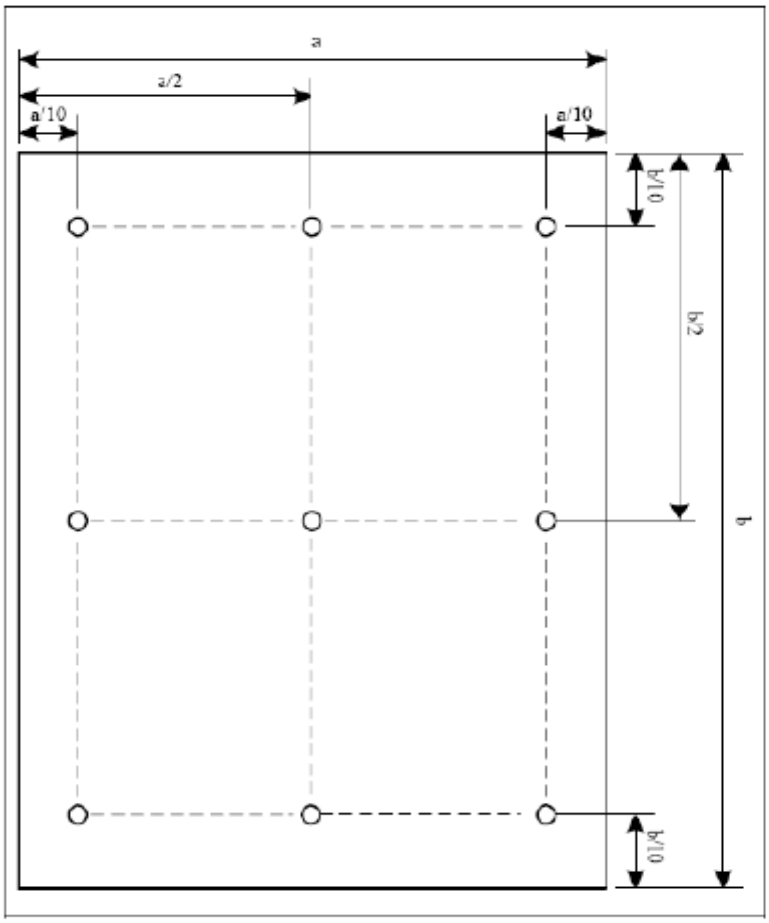
Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=160mA. The LED lifetime could be decreased if operating IL is larger than 160mA. The constant current driving method is suggested.



LED(B/L) CIRCUIT

NOTE 3：Luminance Uniformity of these 9 points is defined as below:

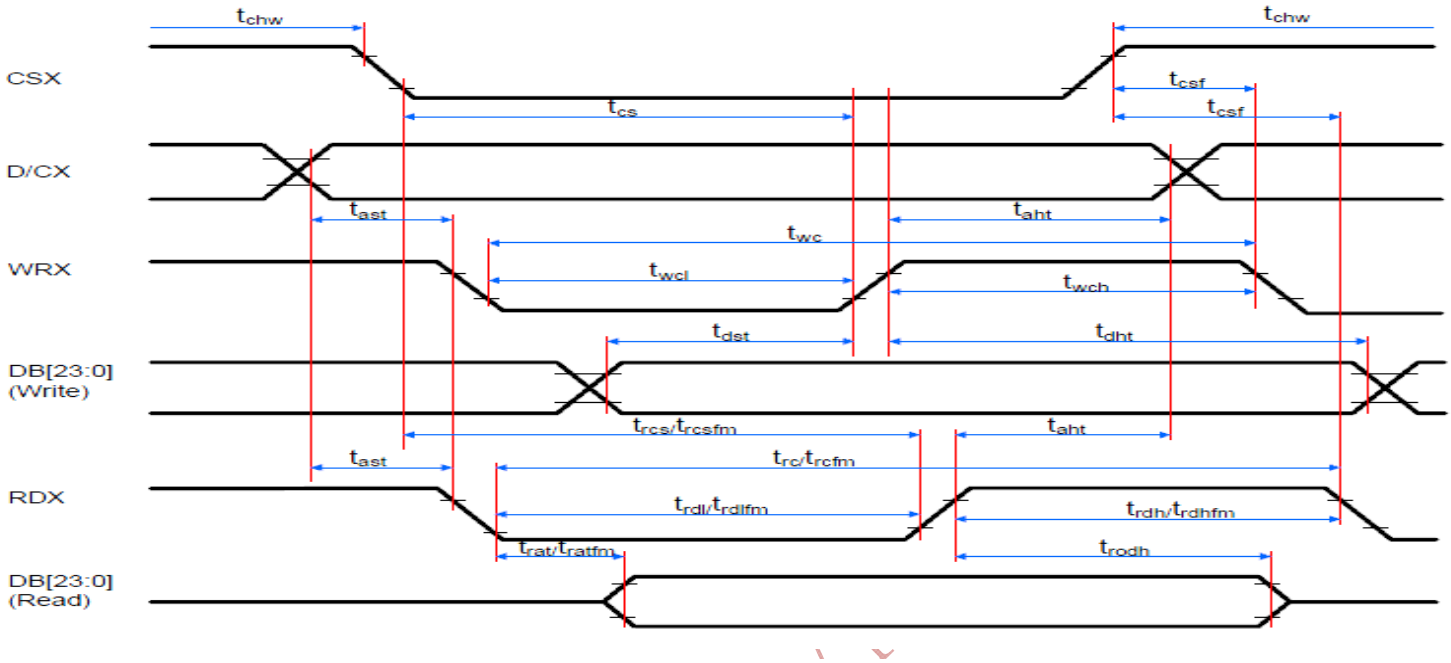


$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

6. AC Characteristic

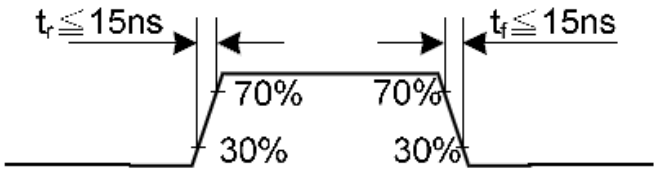
6.1 Display Parallel 8/16-bit Interface Timing Characteristics (8080 system)



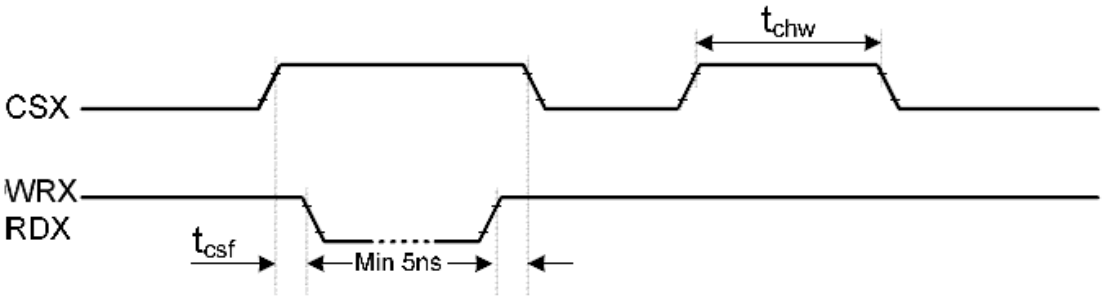
Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	-
	that	Address hold time (Write/Read)	0	-	ns	-
CSX	tchw	CSX "H" pulse width	0	-	ns	-
	tcs	Chip Select setup time (Write)	15	-	ns	-
	trcs	Chip Select setup time (Read ID)	45	-	ns	-
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	-
	tcsf	Chip Select Wait time (Write/Read)	0	-	ns	-
WRX	twc	Write cycle	40	-	ns	-
	twrh	Write Control pulse H duration	15	-	ns	-
	twrl	Write Control pulse L duration	15	-	ns	-
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	When read from Frame Memory
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	When read ID data
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
DB [23:0], DB [17:0], DB [15:0], DB [8:0], DB [7:0]	tdst	Write data setup time	10	-	ns	For maximum, CL=30pF For minimum, CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Notes:

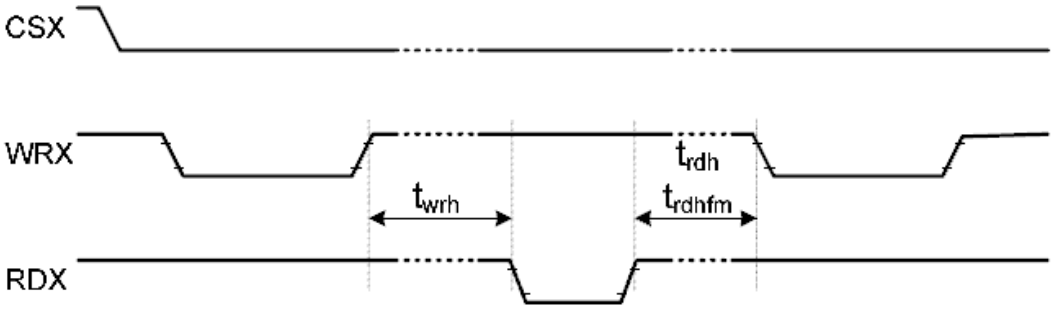
1. Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V
2. Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.
3. Input signal rising time and falling time:



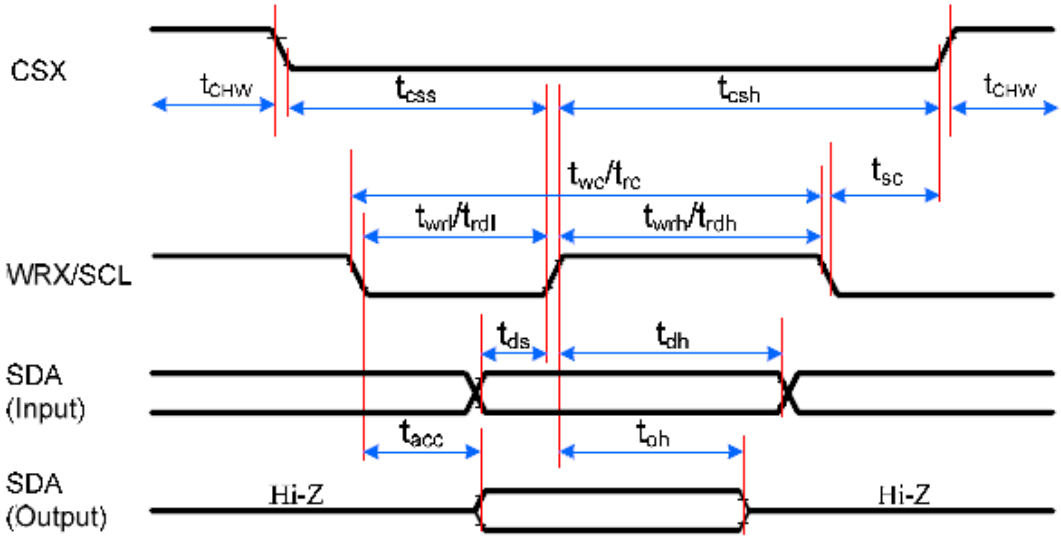
4. The CSX timing:



5. The Write to Read or the Read to Write timing:

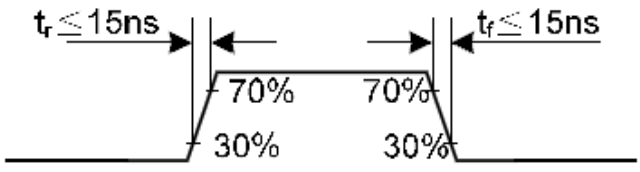


6.2 Display Serial Interface Timing Characteristics (3-line SPI system)

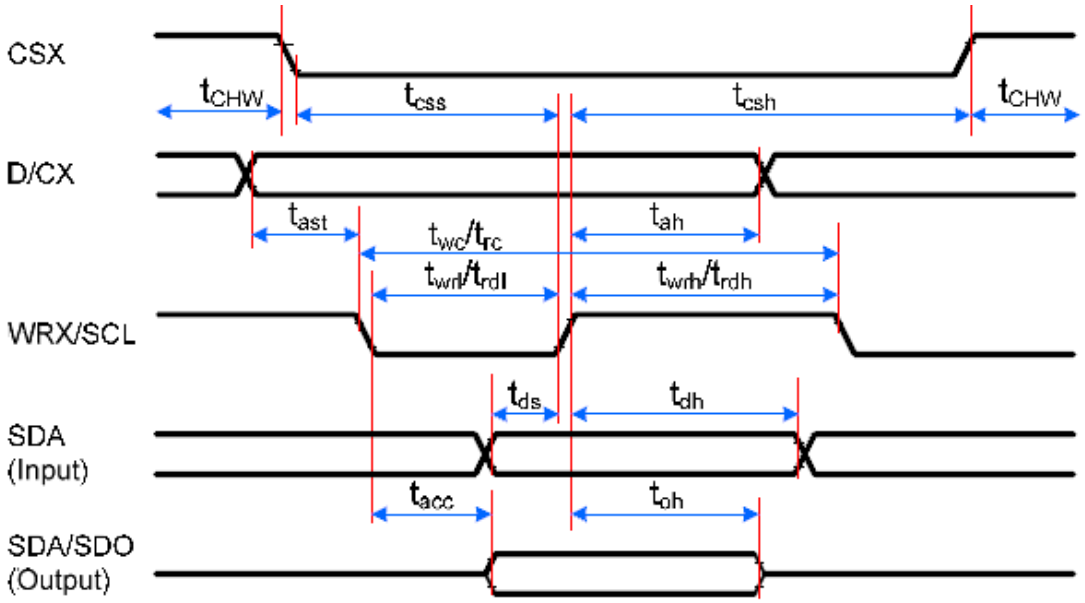


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tsc	SCL-CSX	15	-	ns	
	tchw	CSX H Pulse Width	40	-	ns	
	tcss	Chip select time (Write)	60	-	ns	
	tcsh	Chip select hold time (Read)	65	-	ns	
SCL	twc	Serial Clock Cycle (Write)	66	-	ns	
	twrh	SCL H Pulse Width (Write)	15	-	ns	
	twrl	SCL L Pulse Width (Write)	15	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL H Pulse Width (Read)	60	-	ns	
	trdl	SCL L Pulse Width (Read)	60	-	ns	
SDA (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
	toh	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note: Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.6V, VCI = 2.5V to 3.6V, AGND = DGND = 0V, T = 10+/-0.5ns



6.3Display Serial Interface Timing Characteristics (4-line SPI system)

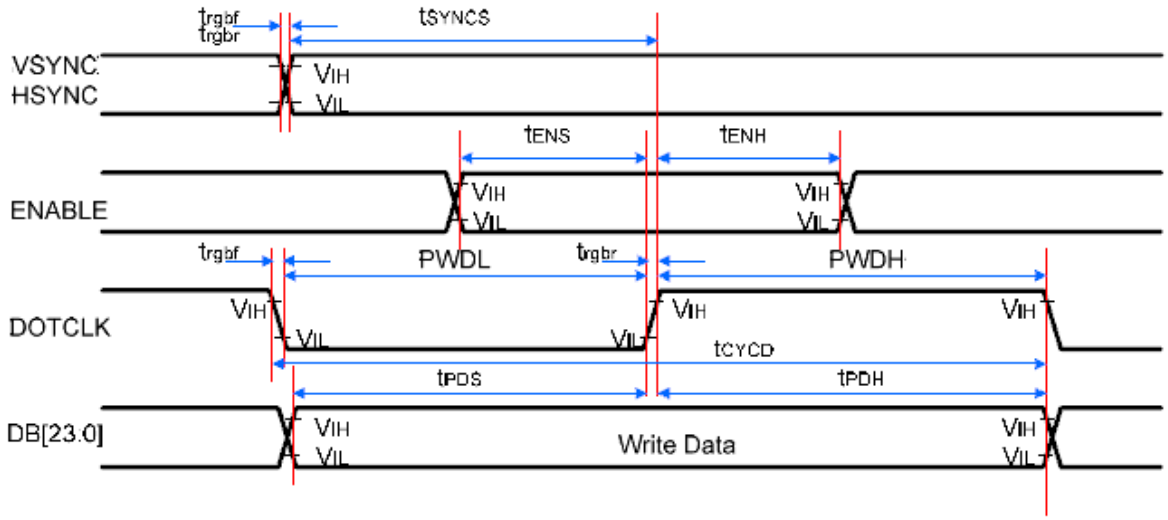


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	15	-	ns	
	tCHW	CS H pulse width	40	-	ns	
SCL	twc	Serial clock cycle (Write)	50	-	ns	
	twrh	SCL H pulse width (Write)	10	-	ns	
	twrl	SCL L pulse width (Write)	10	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL H pulse width (Read)	60	-	ns	
	trdl	SCL L pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
	tod	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Notes:

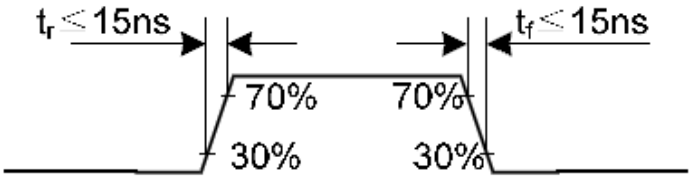
1. Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V, T = 10+/-0.5ns.
2. Does not include signal rising and falling times.

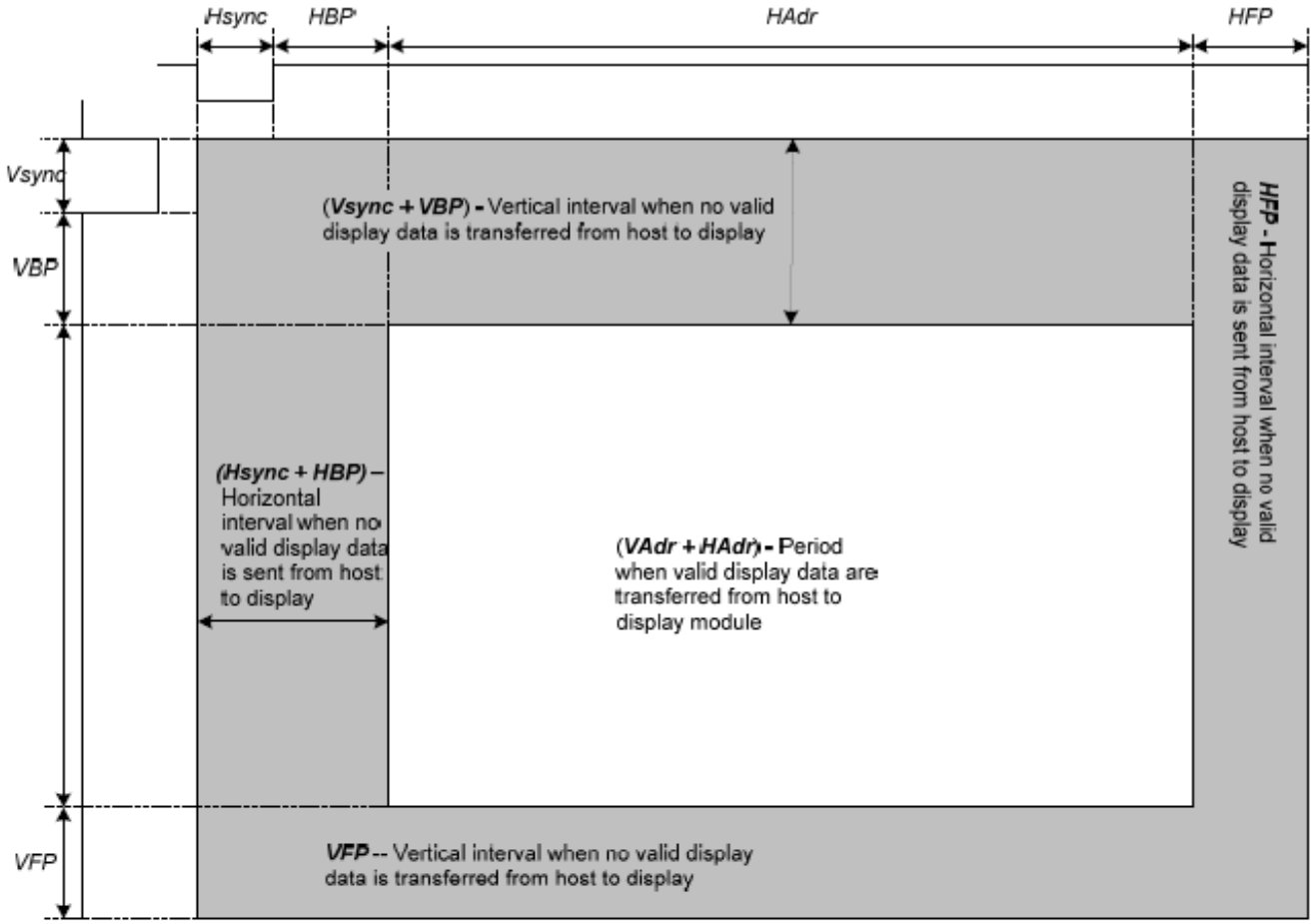
6.4 Parallel RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/ HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
DB [23:0]	t_{POS}	Data setup time	15	-	ns	16-/18-/24-bit bus RGB interface mode
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	20	-	ns	
	PWDL	DOTCLK low-level period	20	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	t_{rgbr}, t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V





Parameters	Symbols	Min.	Typ.	Max.	Units
PCLK Cycle	$PCLK_{CYC}$	100	80	66.6	ns
Horizontal Synchronization	Hsync	3	3	-	PCLK
Horizontal Back Porch	HBP	3	3	-	PCLK
Horizontal Address	HAdr	-	320	-	PCLK
Horizontal Front Porch	HFP	3	3	-	PCLK
Vertical Synchronization	Vsync	2	2	-	Line
Vertical Back Porch	VBP	2	2	-	Line
Vertical Address	VAdr	-	480	-	Line
Vertical Front Porch	VFP	2	2	-	Line
Vertical Frequency(*)		50	60	80	Hz
Horizontal Frequency(*)		-	33	-	KHz
PCLK Frequency(*)		10	12.5	15	MHz

Notes:

1. Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.
2. Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.
3. Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

6.5 Reset Timing Characteristics

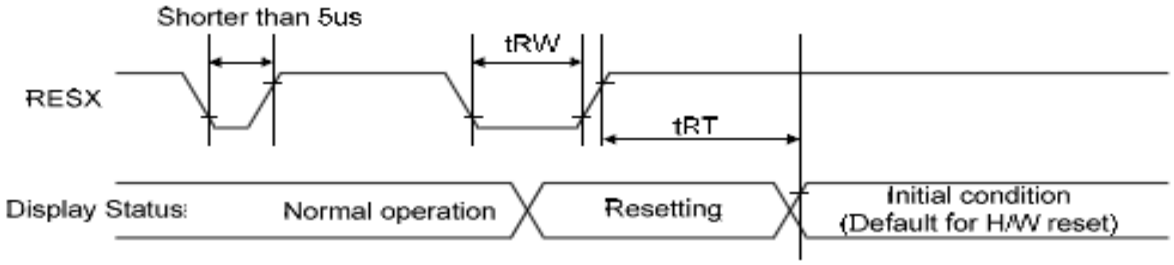


Table 39: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. The reset cancel also includes the required time for loading ID bytes, VCOM setting and other settings from the EEPROM to registers. After a rising edge of RESX, this loading is done within 5 ms after the H/W reset cancel (tRT).
2. According to the Table 40, a spike due to an electrostatic discharge on the RESX line does not cause irregular system reset.

Table 40: Reset Description

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Reset period, the display will be blanked (When Reset starts in the Sleep Out mode, the display will enter the blanking sequence in at least 120 ms. The display remains the blank state in the Sleep In mode.) and then return to the default condition for the Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

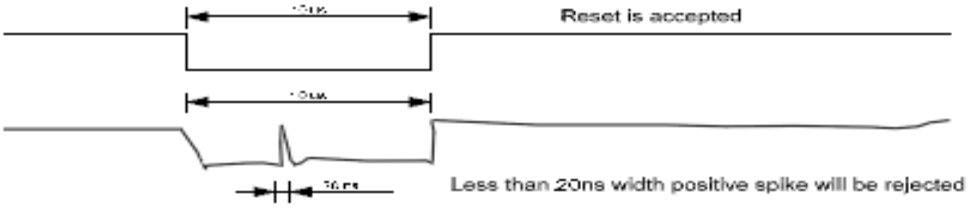


Figure 137: Positive Noise Pulse during Reset Low

7. CTP Specification

7.1 Electrical Characteristics

7.1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	-0.3	3.6	V	1
I/O Digital Voltage	VDDIO	1.8	3.6	V	1
Operating temperature	T_{OP}	-20	+70	℃	-
Storage temperature	T_{ST}	-30	+80	℃	-

NOTES:

1. *If used beyond the absolute maximum ratings, FT6236 may be permanently damaged. It is strongly recommanded that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.*

7.1.2 DC Electrical Characteristics (Ta=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Digital supply voltage	VDD		2.8	3.3	3.6	V	
I/O Digital supply voltage	VDDIO		1.8	3.3	3.6	V	
Normal operation mode Current consumption	I_{opr}	VDD=2.8V Ta=25℃ MCLK= 17.5Mhz	-	4	-	mA	
Monitor mode Current consumption	I_{mon}		-	1.5	-	mA	
Sleep mode Current consumption	I_{slp}			50		uA	
Level input voltage	V_{IH}		$0.7V_{DDIO}$	-	V_{DDIO}	V	
	V_{IL}		-0.3	-	$0.3V_{DDIO}$	V	
Level output voltage	V_{OH}	I_{OH}=-0.1mA	$0.7V_{DDIO}$	-	-	V	
	V_{OL}	I_{OH}=0.1mA	-	-	$0.3V_{DDIO}$	V	

7.2 AC Characteristics

Table 4-1 AC Characteristics of Oscillators

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
OSC clock 1	fosc1	VDDA= 2.8V； Ta=25℃	34.65	35	35.35	MHz	

Table 4-2 AC Characteristics of sensor

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
Sensor acceptable clock	ftx	VDDA= 2.8V； Ta=25℃	0	100	300	KHz	
Sensor output rise time	Ttxr	VDDA= 2.8V； Ta=25℃	-	100	-	nS	
Sensor output fall time	Ttxf	VDDA= 2.8V； Ta=25℃	-	80	-	nS	
Sensor input voltage	Trxi	VDDA= 2.8V； Ta=25℃	-	5	-	V	

7.2.1 I2C Interface

The I2C is always configured in the Slave mode. The data transfer format is shown in Figure4-1:

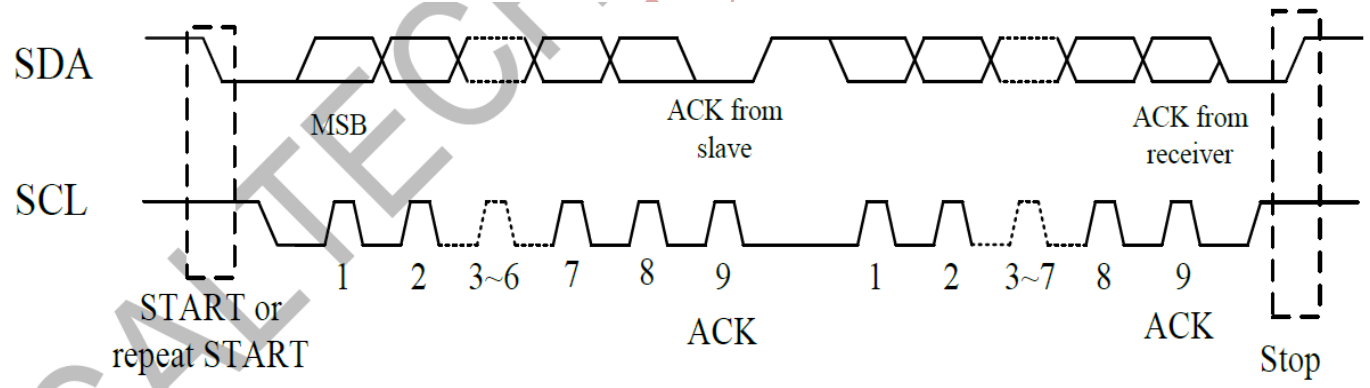


Figure 4-1 I2C Serial Data Transfer Format

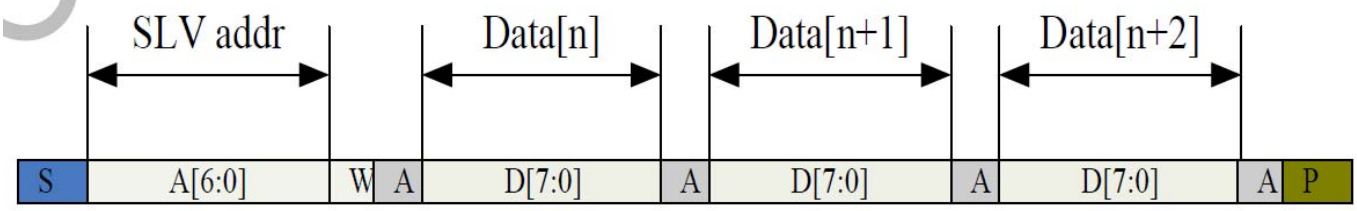


Figure 4-2 I2C master write, slave read

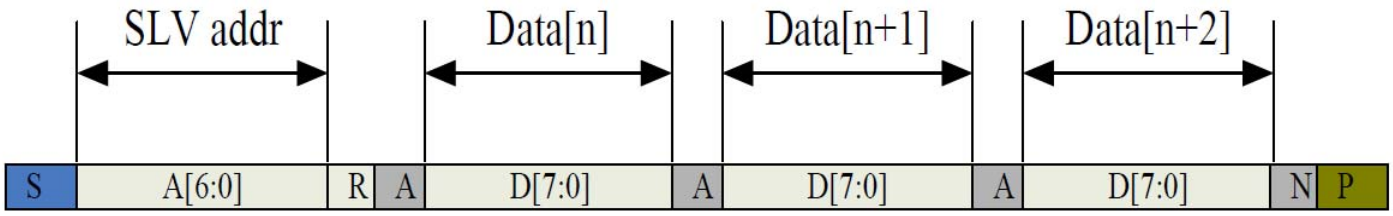


Figure 4-3 I2C master read, slave write

Table4-3 lists the meanings of the mnemonics used in the above figures.

Table 4-3 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/W	READ/WRITE bit, '1' for read, '0'for write
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristcs is shown in Table4-4.

Table 4-4 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	10	400	KHz
Bus free time between a STOP and START condition	4.7	\	us
Hold time (repeated) START condition	4.0	\	us
Data setup time	250	\	ns
Setup time for a repeated START condition	4.7	\	us
Setup Time for STOP condition	4.0	\	us

8.LCD Module Out-Going Quality Level

8.1 VISUAL & FUNCTION INSPECTION STANDARD

8.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

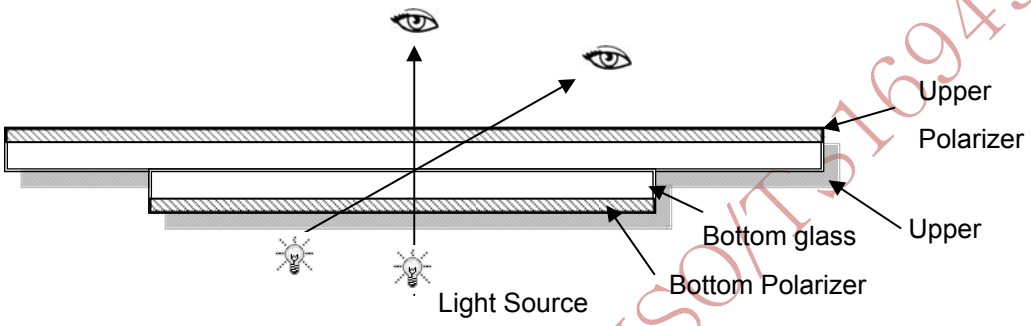
Temperature : 25±5℃

Humidity : 65%±10%RH

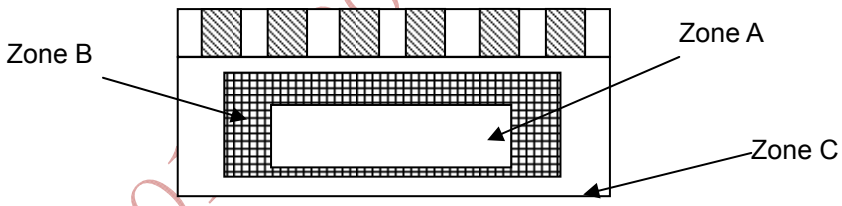
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



8.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer.

8.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class Ⅱ

AQL:

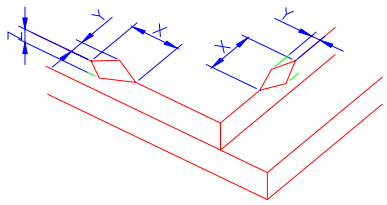
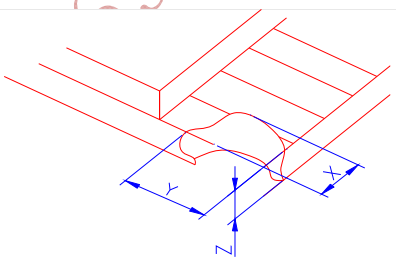
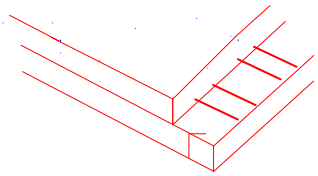
Major defect	Minor defect
0.65	1.5

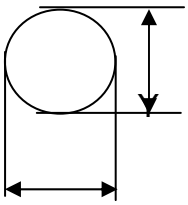
LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Soldering appearance	Good soldering , Peeling off is not allowed.	
6	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

8.1.4 Criteria (Visual)

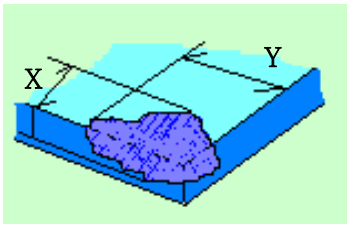
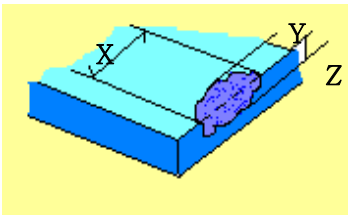
<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken

NOTE:
X: Length
Y: Width
Z: Height
L: Length of ITO,
T: Height of LCD</td><td>(1) The edge of LCD broken</td><td> 
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr>
</table></td></tr>
<tr><td>(2)LCD corner broken</td><td> 
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr>
</table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

<table>
<tr><th>Number</th><th>Items</th><th>Criteria (mm)</th></tr>
<tr><td>2.0</td><td>Spot defect
 
X
Φ=(X+Y)/2</td><td>① light dot（LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain）
<table>
<tr><th rowspan="2">Zone
Size (mm)</th><th colspan="3">Accep able Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.10</td><td colspan="2">Ignore</td><td rowspan="4">Ignor</td></tr>
<tr><td>0.10<Φ≤0.20</td><td colspan="2">3(distance≧10mm)</td></tr>
<tr><td>0.20<Φ≤0.25</td><td colspan="2">2</td></tr>
<tr><td>Φ＞0.25</td><td colspan="2">0</td></tr>
</table>
②Dim spot（LCD/TP/Polarizer dim dot, light leakage、dark spot）
<table>
<tr><th rowspan="2">Zone
Size (mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.10<Φ≤0.20</td><td colspan="2">3(distance≧10mm)</td></tr>
<tr><td>0.20<Φ≤0.30</td><td colspan="2">2</td></tr>
<tr><td>Φ＞0.30</td><td colspan="2">0</td></tr>
</table>
③ Polarizer accidented spot
<table>
<tr><th rowspan="2">Zone
Size (mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.2</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.3<Φ≤0.5</td><td colspan="2">2(distance≧10mm)</td></tr>
<tr><td>Φ>0.5</td><td colspan="2">0</td></tr>
</table></td></tr>
<tr><td></td><td>Line defect (LCD/TP /Polarizer black/white line, scratch, stain)</td><td>
<table>
<tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(mm</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.03</td><td>Igno e</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.03<W≤0.05</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.05<W≤0.08</td><td>L≤2.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.08<W</td><td colspan="4">Define as spot defect</td></tr>
</table></td></tr>
</table>

<table>
<tr><td>3.0</td><td>Polarizer Bubble</td><td>
<table>
<tr><td rowspan="2">Zone
Size (mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.2</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.2<Φ≤0.4</td><td colspan="2">3(distance≧10 m)</td></tr>
<tr><td>0.4<Φ≤0.6</td><td colspan="2">2</td></tr>
<tr><td>0.6<Φ</td><td colspan="2">0</td></tr>
</table>
</td></tr>
<tr><td>4.0</td><td>SMT</td><td>According to IPC-A-610C class Ⅱ standard . Function defect and missing part are major defect ,the others are minor defect.</td></tr>
</table>

<table>
<tr><td rowspan="2"></td><td rowspan="2"></td><td>TP bubble/ accidented spot</td><td>
<table>
<tr><td rowspan="2">Size Φ(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.1<Φ≤0.25</td><td colspan="2">3 (distance≧</td></tr>
<tr><td>0.25<Φ≤0.3</td><td colspan="2">2</td></tr>
<tr><td>0.3<Φ</td><td colspan="2">0</td></tr>
</table>
</td></tr>
<tr><td>Assembly deflection</td><td>beyond the edge of backlight ≤0.15mm</td></tr>
</table>

<table>
<tr><td>5.0</td><td>TP Related</td><td>Newton Ring</td><td>Newton Ring area>1/3 TP area NG
Newton Ring area≤1/3 TP area OK</td><td>  </td></tr>
<tr><td></td><td></td><td>TP corner broken
X：length
Y：width
Z：height</td><td><table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>X≤3.0mm</td><td>Y≤3.0mm</td><td>Z<LCD thicknes</td></tr></table>*
Circuitry broken is not allowed.</td><td>  </td></tr>
<tr><td></td><td></td><td>TP edge broken
X：length
Y：width
Z：height</td><td><table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>X≤6.0mm</td><td>Y≤2.0mm</td><td>Z<LCD thicknes</td></tr></table>* Circuitry broken is not allowed.</td><td>  </td></tr>
</table>

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

9. Reliability Test Result

9.1 Condition

Item	Condition	Sample Size	Test Result	Note
Low Temperature Operating Life test	-20℃, 96HR	3ea	pass	-
Thermal Humidity Operating Life test	70℃90%RH, 96HR	3ea	pass	-
Temperature Cycle ON/OFF test	-20℃ ↔ 70℃, ON/OFF, 20CYC	3ea	pass	(1)
High Temperature Storage test	80℃, 96HR	3ea	pass	-
Low Temperature Storage test	－30℃, 96HR	3ea	pass	-
ESD test	150pF, 330Ω , ±6KV(Contact)/± 8KV(Air), 5 points/panel, 10 times/point	3ea	pass	
Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours	3ea	pass	
Box Drop Test	1 Corner 3 Edges 6 faces, 66㎝(MEDIUM BOX)	1box	pass	-

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds

10. Cautions and Handling Precautions

10.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
(8) Protect the module from static; it may cause damage to the CMOS ICs.
(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
(10) Do not disassemble the module.
(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
(12) Pins of I/F connector shall not be touched directly with bare hands.
(13) Do not connect, disconnect the module in the “Power ON” condition.
(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence &6.2 Power Off Sequence

10.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
(2) Do not store the TFT-LCD module in direct sunlight.
(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

11. Packing

----TBD----------